SN74LVC125A 具有三态输出的四路总线缓冲门

1 特性

- 三态输出
- 为所有 4 个缓冲器提供单独的 $\overline{OE}$
- 工作电压范围为 1.65V 至 3.6V
- 额定工作温度范围为 –40°C 至 85°C 以及 –40°C 至 125°C
- 输入电压高达 5.5V
- 电压为 3.3V 时，t_{pd} 最大值为 4.8ns
- V_{OLP}（输出接地反弹）典型值小于 0.8V（V_{CC} = 3.3V、T_A = 25°C）
- V_{OHV}（输出 V_{OH} 下冲）典型值大于 2V（V_{CC} = 3.3V、T_A = 25°C 时）
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 线缆调制解调器终端系统
- IP 电话：有线和无线
- 光学模块
- 光纤网络：
  - EPON 或光纤视频
- 点对点微波回程
- 电源：直流/直流通信电源模块：
  - 模拟或数字
- 专用分支交换机 (PBX)
- TETRA 基站
- 电信基带单元
- 电信方舱：
  - 滤波器单元
  - 配电单元 (PDU)
  - 电源监控单元 (PMU)
  - 无线电池监控
  - 远程电动倾斜单元 (RET)
  - 远程射频单元 (RRU)
  - 塔顶放大器 (TMA)
- 矢量信号分析仪和发生器
- 视频会议：基于 IP 的高清视频
- WiMAX 和无线基础设施设备
- 无线通信测试仪
- xDSL 调制解调器和 DSLAM

3 说明

这款四路总线缓冲门可在 1.65V 至 3.6V V_{CC} 下运行。

SN74LVC125A 器件具有提供三态输出的独立线路驱动器。当每个输出的相关输出使能 ($\overline{OE}$) 输入为高电平时，输出被禁用。

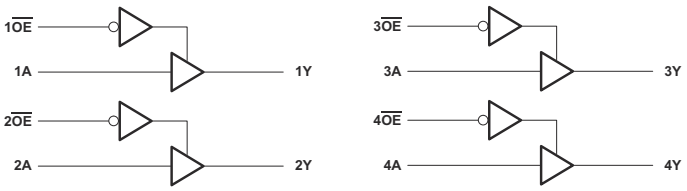
为了确保加电或断电期间的高阻抗状态，$\overline{OE}$ 应通过一个上拉电阻器被连接至 V_{CC}；该电阻器的最小值由驱动器的电流吸收能力来决定。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将该器件用作转换器。

封装信息

器件型号	封装(1)	封装尺寸(2)	封装尺寸(3)
SN74LVC125A	BQA（WQFN，14）	3mm × 2.5mm	3mm × 2.5mm
	D（SOIC，14）	8.6mm × 6mm	8.65mm × 3.91mm
	DB（SSOP，14）	6.20mm × 7.8mm	6.20mm x 5.30mm
	NS（SOP，14）	10.2mm × 7.8mm	10.30mm x 5.30mm
	PW（TSSOP，14）	5.00mm x 6.4mm	5.00mm × 4.40mm
	RGY（VQFN，14）	3.50mm × 3.50mm	3.50mm × 3.50mm

(1) 更多相关信息，请参阅第 11 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。



简化版原理图

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 引脚配置和功能

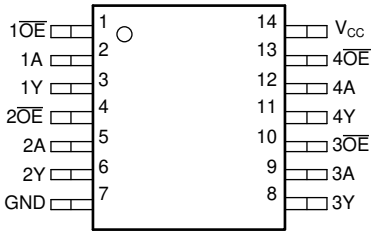


图 4-1. D、DB、NS 或 PW 封装（顶视图）

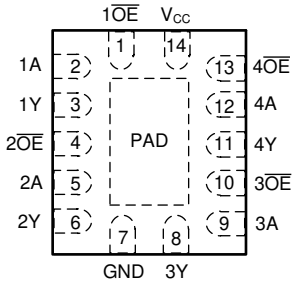


图 4-2. BQA 或 RGY 封装（顶视图）

表 4-1. 引脚功能

引脚		I/O[1]	说明
名称	编号		
$1\overline{OE}$	1	输入	输出使能
1A	2	输入	输入 A
1Y	3	输出	输出 Y
$2\overline{OE}$	4	输入	输出使能
2A	5	输入	输入 A
2Y	6	输出	输出 Y
GND	7	—	地
3Y	8	输出	输出 Y
3A	9	输入	输入 A
$3\overline{OE}$	10	输入	输出使能
4Y	11	输出	输出 Y
4A	12	输入	输入 A
$4\overline{OE}$	13	输入	输出使能
V_{CC}	14	—	正电源

(1) I = 输入，O = 输出，I/O = 输入或输出，G = 地，P = 电源

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5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	6.5	V
V_I	输入电压范围(2)		-0.5	6.5	V
V_O	输出电压范围(2) (3)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-50	mA
I_{OK}	输出钳位电流	V_O < 0		-50	mA
I_O	持续输出电流			±50	mA
	通过 V_{CC} 或 GND 的持续电流			±100	mA
P_{tot}	功率耗散	T_A = -40°C 至 125°C(4) (5)		500	mW
T_{stg}	贮存温度范围		-65	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些仅为应力等级，并不表示器件在这些条件下以及在*节 5.3* 以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
(3) V_{CC} 的值在*节 5.3* 表中提供。
(4) 对于 D 封装：在 70°C 以上时，P_{tot} 值以 8mW/K 的幅度线性降额。
(5) 对于 DB、NS 和 PW 封装：在 60°C 以上时，P_{tot} 值以 5.5mW/K 的幅度线性降额。

5.2 ESD 等级

参数		定义	值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准，所有引脚(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101，所有引脚(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 支持在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 支持在标准 ESD 控制流程下安全生产。

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5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			T_A = 25°C		– 40°C 至 85°C		-40°C 至 125°C		单位
			最小值	最大值	最小值	最大值	最小值	最大值	
V_{CC}	电源电压	运行	1.65	3.6	1.65	3.6	1.65	3.6	V
		仅数据保留	1.5		1.5		1.5		
V_{IH}	高电平输入电压	V_{CC} = 1.65V 至 1.95V	0.65 × V_{CC}		0.65 × V_{CC}		0.65 × V_{CC}		V
		V_{CC} = 2.3V 至 2.7V	1.7		1.7		1.7		
		V_{CC} = 2.7V 至 3.6V	2		2		2		
V_{IL}	低电平输入电压	V_{CC} = 1.65V 至 1.95V		0.35 × V_{CC}		0.35 × V_{CC}		0.35 × V_{CC}	V
		V_{CC} = 2.3V 至 2.7V		0.7		0.7		0.7	
		V_{CC} = 2.7V 至 3.6V		0.8		0.8		0.8	
V_I	输入电压		0	5.5	0	5.5	0	5.5	V
V_O	输出电压		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 1.65V		-4		-4		-4	mA
		V_{CC} = 2.3V		-8		-8		-8	
		V_{CC} = 2.7V		-12		-12		-12	
		V_{CC} = 3V		-24		-24		-24	
I_{OL}	低电平输出电流	V_{CC} = 1.65V		4		4		4	mA
		V_{CC} = 2.3V		8		8		8	
		V_{CC} = 2.7V		12		12		12	
		V_{CC} = 3V		24		24		24	
$\Delta t/\Delta v$	输入转换上升或下降速率			8		8		8	ns/V

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢或悬空的影响*，文献编号 SCBA004。

5.4 热性能信息

热性能指标(1)		SN74LVC125A						单位
		BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	102.3	127.8	140.4	123.8	150.8	92.1	°C/W

(1) 有关新旧热指标的更多信息，请参阅半导体和 IC 封装热指标应用手册。

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5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			-40°C 至 85°C		-40°C 至 125°C		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = –100 μA	1.65V 至 3.6V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.3		V
	I_{OH} = –4mA	1.65V	1.29			1.2		1.05		
	I_{OH} = –8mA	2.3V	1.9			1.7		1.55		
	I_{OH} = –12mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
	I_{OH} = –24mA	3V	2.3			2.2		2		
V_{OL}	I_{OL} = 100 μA	1.65V 至 3.6V			0.1		0.2		0.3	V
	I_{OL} = 4mA	1.65V			0.24		0.45		0.6	
	I_{OL} = 8mA	2.3V			0.3		0.7		0.75	
	I_{OL} = 12mA	2.7V			0.4		0.4		0.6	
	I_{OL} = 24mA	3V			0.55		0.55		0.8	
I_I	V_I = 5.5V 或 GND	3.6V			±1		±5		±20	μA
I_{OZ}	V_O = V_{CC} 或 GND	3.6V			±1		±10		±20	μA
I_{CC}	V_I = V_{CC} 或 GND，I_O = 0	3.6V			1		10		40	μA
ΔI_{CC}	一个输入电压为 V_{CC} – 0.6V，其他输入电压为 V_{CC} 或 GND	2.7V 至 3.6V			500		500		5000	μA
C_i	V_I = V_{CC} 或 GND	3.3V		5						pF

5.6 开关特性

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	V_{CC}	T_A = 25°C			-40°C 至 85°C		-40°C 至 125°C		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	1.8V ± 0.15V	1	4.5	11.8	1	12.3	1	13.8	ns
			2.5V ± 0.2V	1	2.7	5.8	1	6.3	1	8.4	
			2.7V	1	3	5.3	1	5.5	1	7	
			3.3V ± 0.3V	1	2.5	4.6	1	4.8	1	6	
t_{en}	$\overline{OE}$	Y	1.8V ± 0.15V	1	4.3	13.8	1	14.3	1	15.8	ns
			2.5V ± 0.2V	1	2.7	6.9	1	7.4	1	9.5	
			2.7V	1	3.3	6.4	1	6.6	1	8.5	
			3.3V ± 0.3V	1	2.4	5.2	1	5.4	1	7	
t_{dis}	$\overline{OE}$	Y	1.8V ± 0.15V	1	4.3	10.6	1	11.1	1	12.6	ns
			2.5V ± 0.2V	1	2.2	5.1	1	5.6	1	7.7	
			2.7V	1	2.5	4.8	1	5	1	6.5	
			3.3V ± 0.3V	1	2.4	4.4	1	4.6	1	6	
$t_{sk(o)}$			3.3V ± 0.3V					1		1.5	ns

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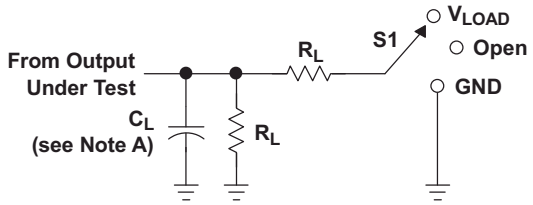
5.7 工作特性

T_A = 25°C

参数		测试条件	V_{CC}	典型值	单位
C_{pd}	每个栅极的功率耗散电容	f = 10MHz	1.8V	7.4	pF
			2.5V	11.3	
			3.3V	15	

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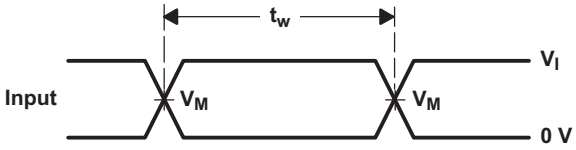
6 参数测量信息



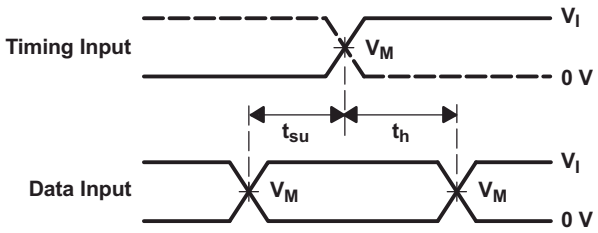
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

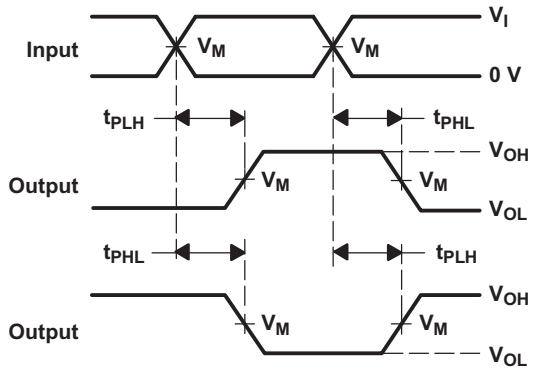
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



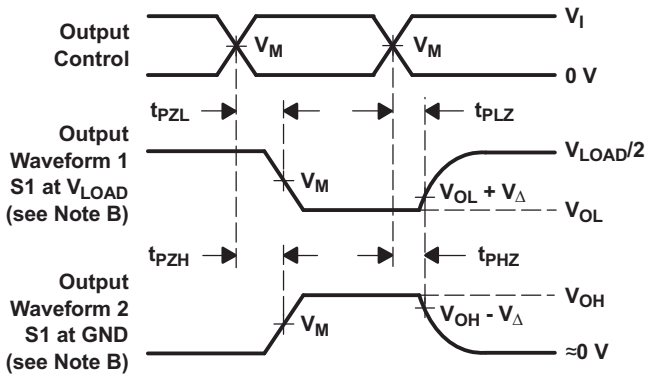
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 6-1. 负载电路和电压波形

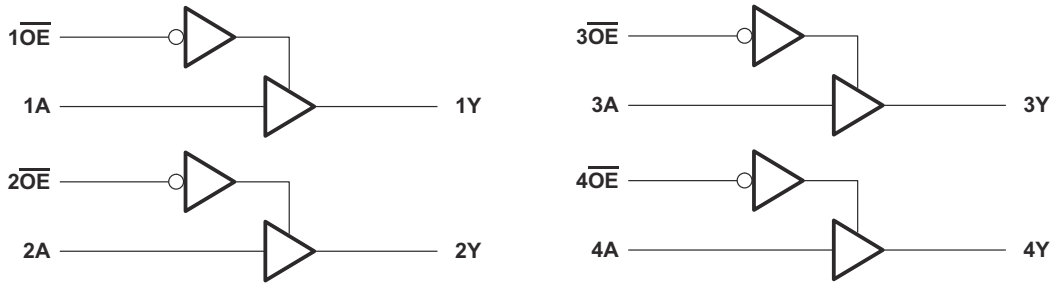
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7 详细说明

7.1 概述

SN74LVC125A 器件是一款四通道总线缓冲门，具有独立的线路驱动器和三态输出。当每个输出的相关输出使能 ($\overline{OE}$) 输入为高电平时，输出被禁用。当 $\overline{OE}$ 为低电平时，相应的逻辑门会将来自 A 输入的数据传递到 Y 输出。为确保在上电或下电期间均处于高阻态，应将 OE 通过一个上拉电阻连接至 V_{CC}；该电阻的最小阻值取决于驱动器的拉电流能力。

7.2 功能方框图



7.3 特性说明

- 宽工作电压范围
  - 可在 1.65V 至 5.5V 范围内工作
- 支持升降压转换
- 输入电压高达 5.5V

7.4 器件功能模式

表 7-1. 功能表

输入		输出
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 典型应用

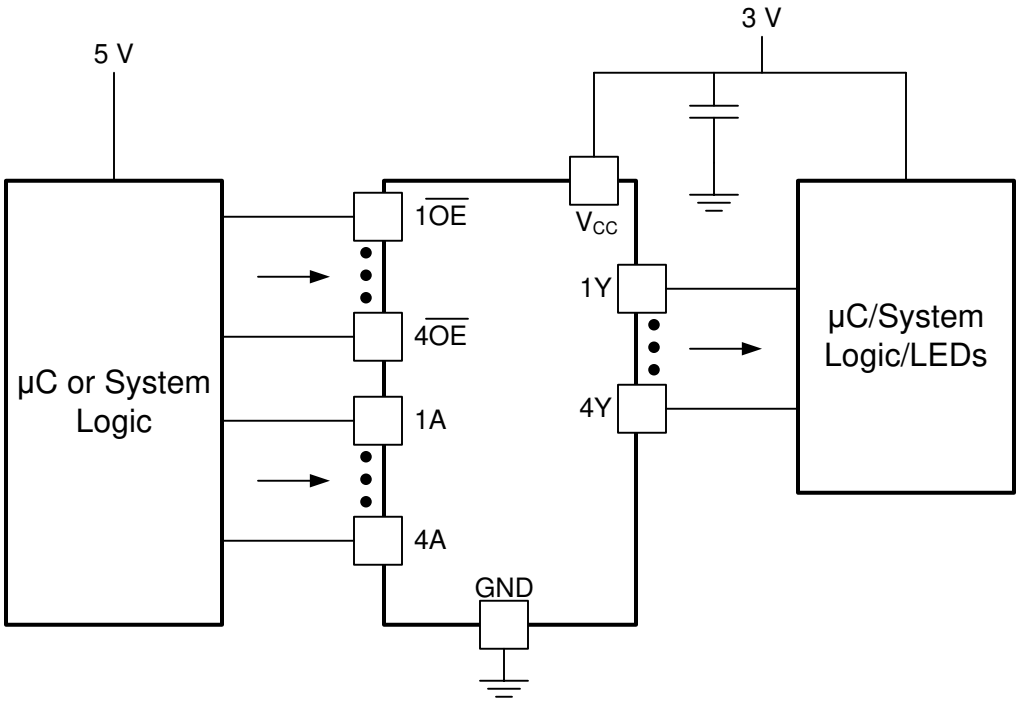


图 8-1. 典型应用原理图

8.1.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

8.1.2 详细设计过程

1. 建议的输入条件：
   - 有关上升时间和下降时间规格，请参阅 *节 5.3* 表中的 ($\Delta t/\Delta V$)。
   - 有关指定的高电平和低电平，请参阅 *节 5.3* 表中的 (V_{IH} 和 V_{IL})。
   - 输入可耐受过压，因此可在任何有效的 *VCC* 下高达 *节 5.3* 表中的 (V_I 最大值)。
2. 建议的输出条件：
   - 每路输出的负载电流不应超过 (I_O 最大值)，且不能超过该器件的总电流 (通过 V_{CC} 或 GND 的持续电流)。这些限值位于 *节 5.1* 表中。
   - 输出不应被拉至高于 V_{CC}。
   - 如果用户希望降低输出边沿信号的速度或限制输出电流，则可以在输出端使用串联电阻器。

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8.1.3 应用曲线

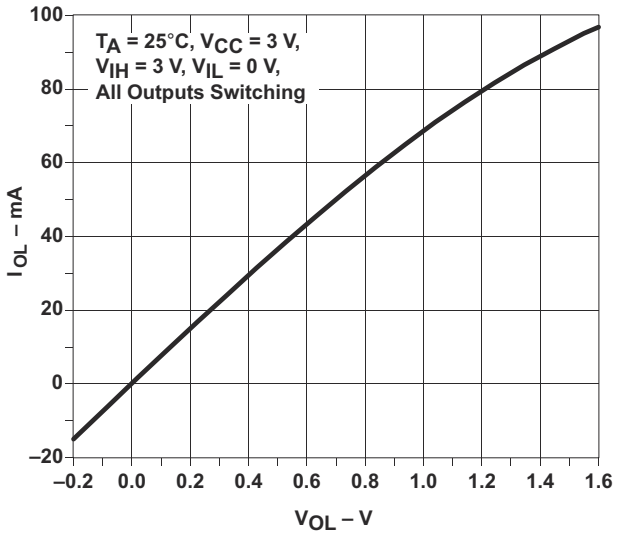


图 8-2. 输出驱动电流 (I_{OL}) 与低电平输出电压 (V_{OL}) 间的关系

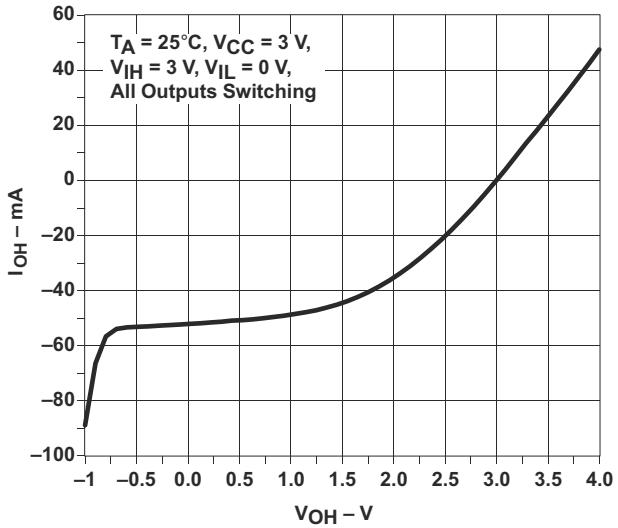


图 8-3. 输出驱动电流 (I_{OH}) 与高电平输出电压 (V_{OH}) 间的关系

8.2 电源相关建议

电源可以是 *节 5.3* 表中最小和最大电源电压额定值之间的任意电压。

每个 V_{CC} 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 µf；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 0.01 µf 或 0.022 µf。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µf 和 1 µf 通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

8.3 布局

8.3.1 布局指南

当使用多位逻辑器件时，输入不应悬空。在许多情况下，数字逻辑器件的功能或部分功能未被使用。例如，在仅使用三输入与门的两个输入，或仅使用 4 个缓冲门中的 3 个时。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的运行状态。

图 8-4 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应为任何特定未使用输入施加的逻辑电平取决于器件的功能。通常，将这些输入连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。

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8.3.2 布局示例

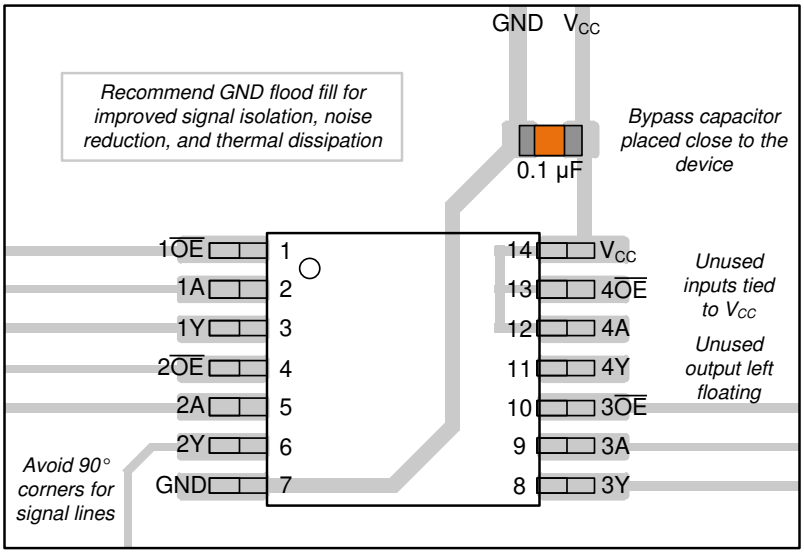


图 8-4. SN74LVC125A 的示例布局

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9 器件和文档支持

9.1 文档支持

9.1.1 相关文档

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 9-1. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
SN74LVC125A	点击此处	点击此处	点击此处	点击此处	点击此处

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

Changes from Revision S (May 2024) to Revision T (September 2024)	Page
• 将 D 封装的热性能指标 R θ JA 的值从 86 更新为 127.8，所有值均以 °C/W 为单位	5

Changes from Revision R (February 2024) to Revision S (May 2024)	Page
• 更新了 R θ JA 值：DB = 96 更新至 140.4，NS = 76 更新至 123.8，PW = 113 更新至 150.8，RGY = 47 更新至 92.1；更新了 DB、NS、PW 和 RGY 封装的 R θ JC(top)、R θ JB、ΨJT、ΨJB 和 R θ JC(bot)，所有值均以 °C/W 为单位	5

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC125ABQAR	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LVC125ABQAR.A	Active	Production	WQFN (BQA) | 14	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LVC125AD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125AD.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADBR	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADBR.A	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADBR.B	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADBRG4	Active	Production	SSOP (DB) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADE4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRE4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG3	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG3.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG4.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADT.B	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADTG4	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANS.B	Active	Production	SOP (NS) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSR.B	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSRG4	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSRG4.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSRG4.B	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125APW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC125APW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWE4	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWG4	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRE4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG3	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LC125A
SN74LVC125APWRG3.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG3.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG4.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG4.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWT	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWT.B	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWTE4	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWTG4	Active	Production	TSSOP (PW) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ARGYR	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC125A
SN74LVC125ARGYR.A	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC125A
SN74LVC125ARGYR.B	Active	Production	VQFN (RGY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC125A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC125A :

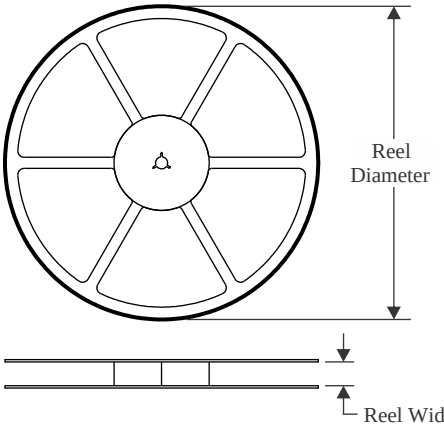
- Automotive : SN74LVC125A-Q1
- Enhanced Product : SN74LVC125A-EP

NOTE: Qualified Version Definitions:

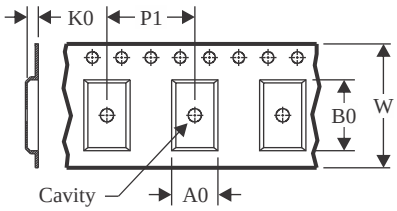
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

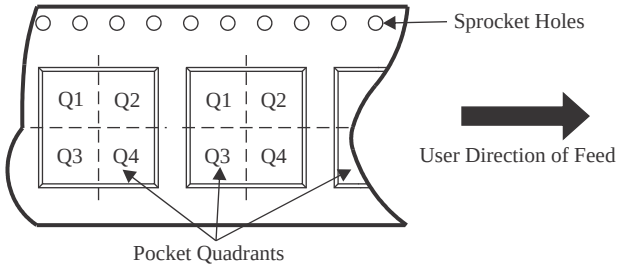


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

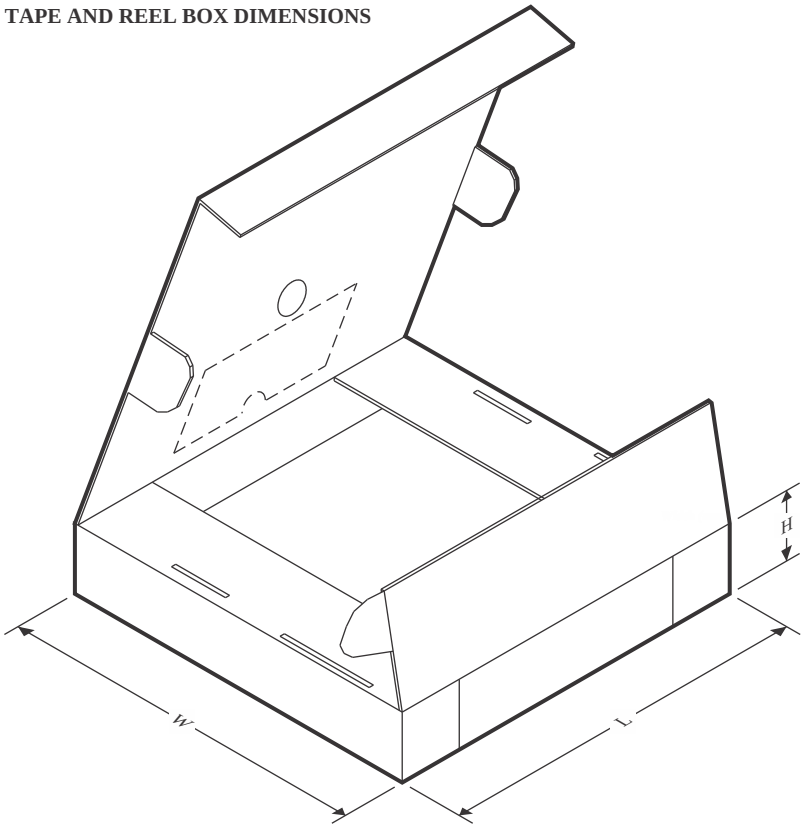


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC125ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC125ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ADRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74LVC125ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC125ANSRG4	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74LVC125APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC125APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

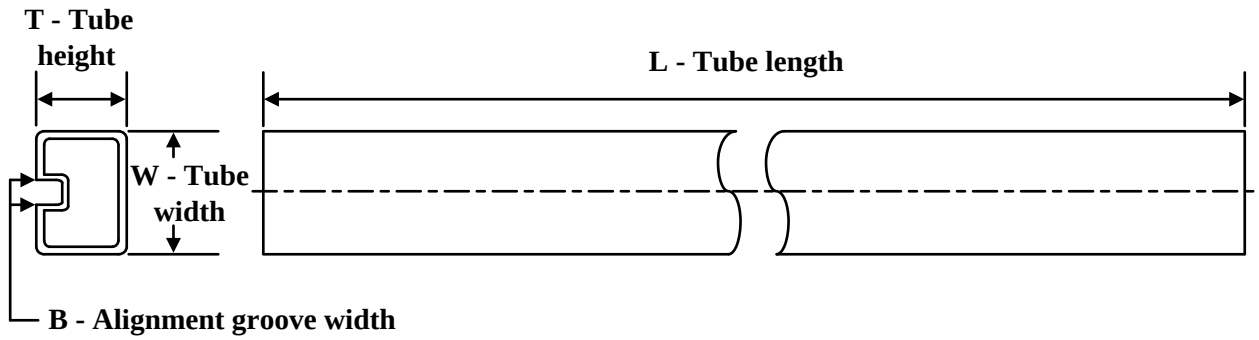


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC125ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC125ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVC125ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC125ADRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC125ADRG4	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC125ADRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC125ADT	SOIC	D	14	250	213.0	191.0	35.0
SN74LVC125ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC125ANSRG4	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC125APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC125APWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74LVC125APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LVC125APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC125APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC125APWRG3	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74LVC125APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC125APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC125APWT	TSSOP	PW	14	250	353.0	353.0	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC125ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC125AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125ADE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125ANS.B	NS	SOP	14	50	530	10.5	4000	4.1
SN74LVC125APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC125APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC125APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC125APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

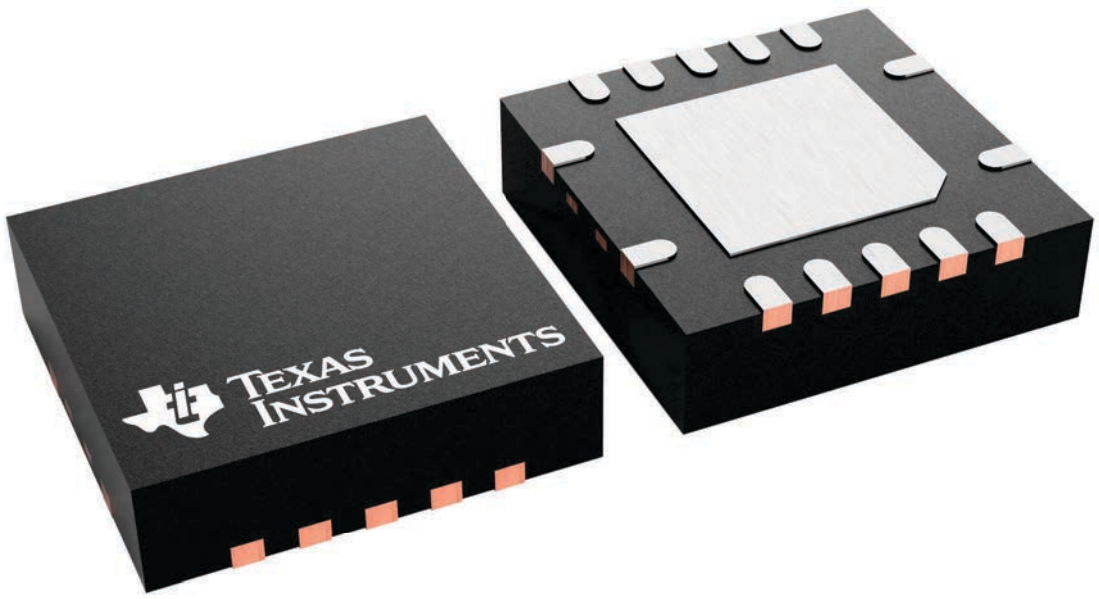
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



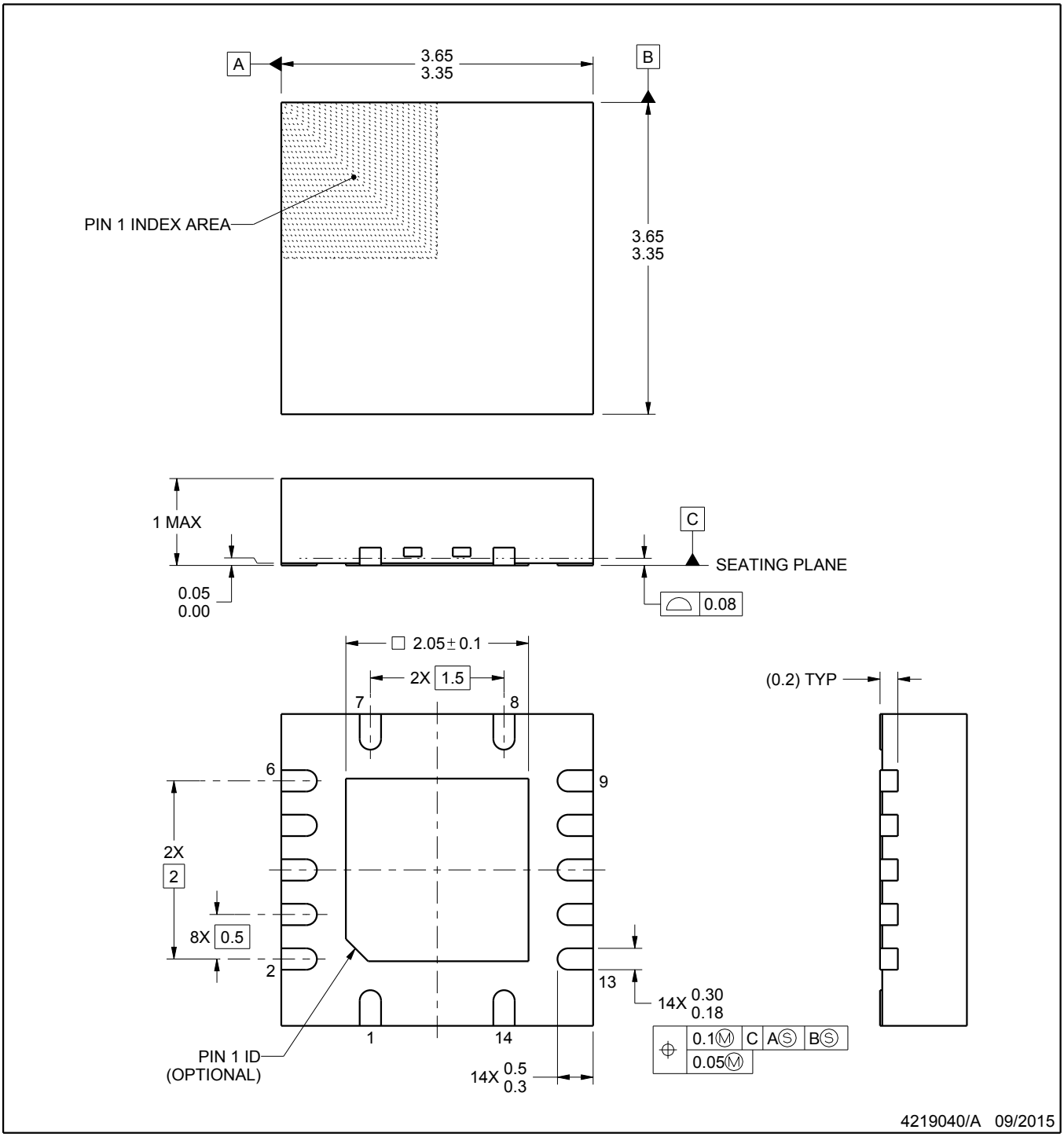
4231541/A

PACKAGE OUTLINE

RGY0014A

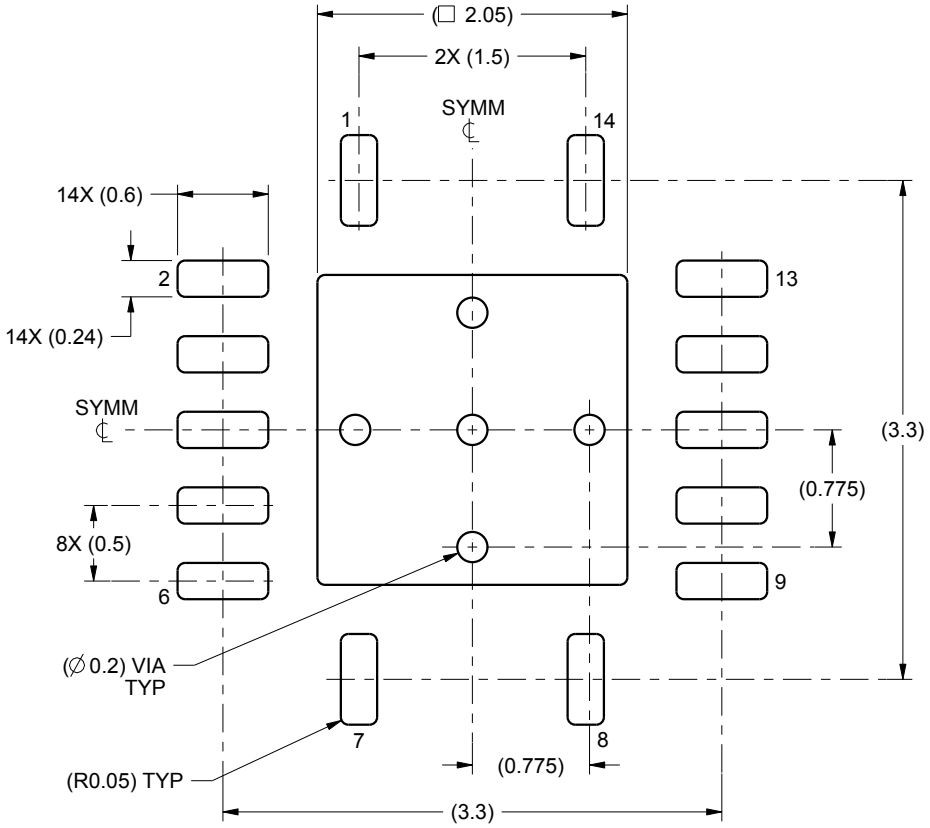
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

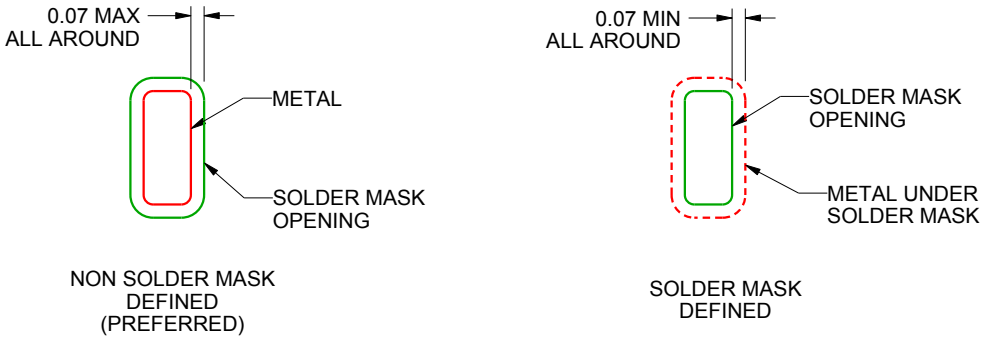


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

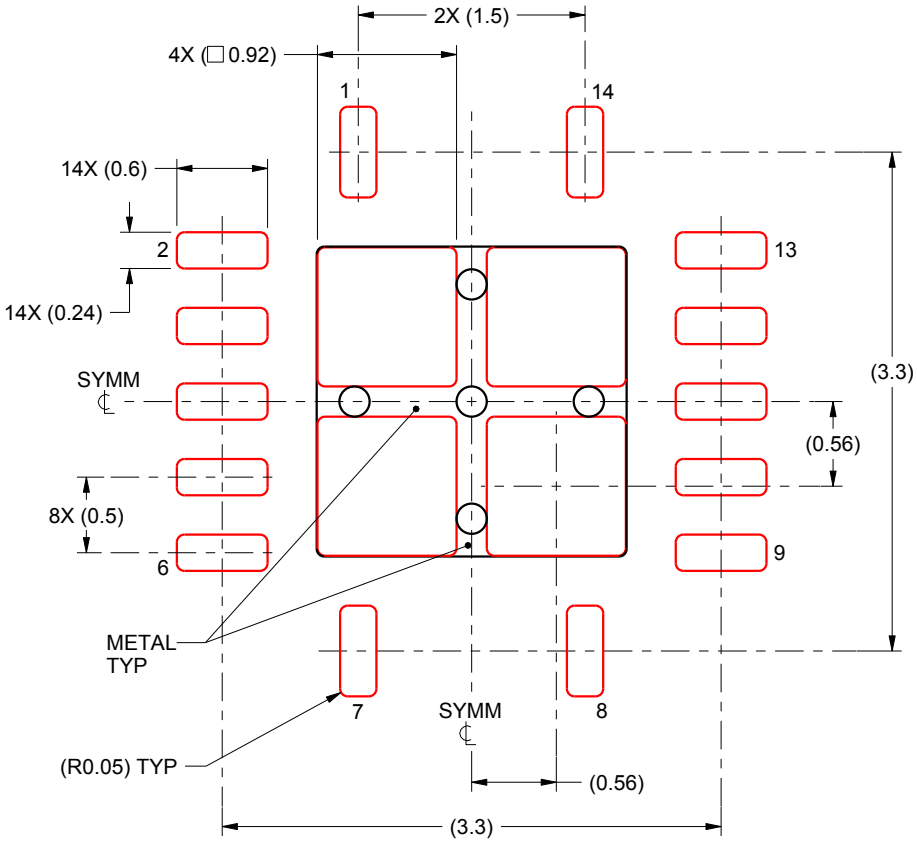


SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



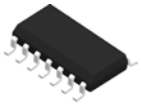
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

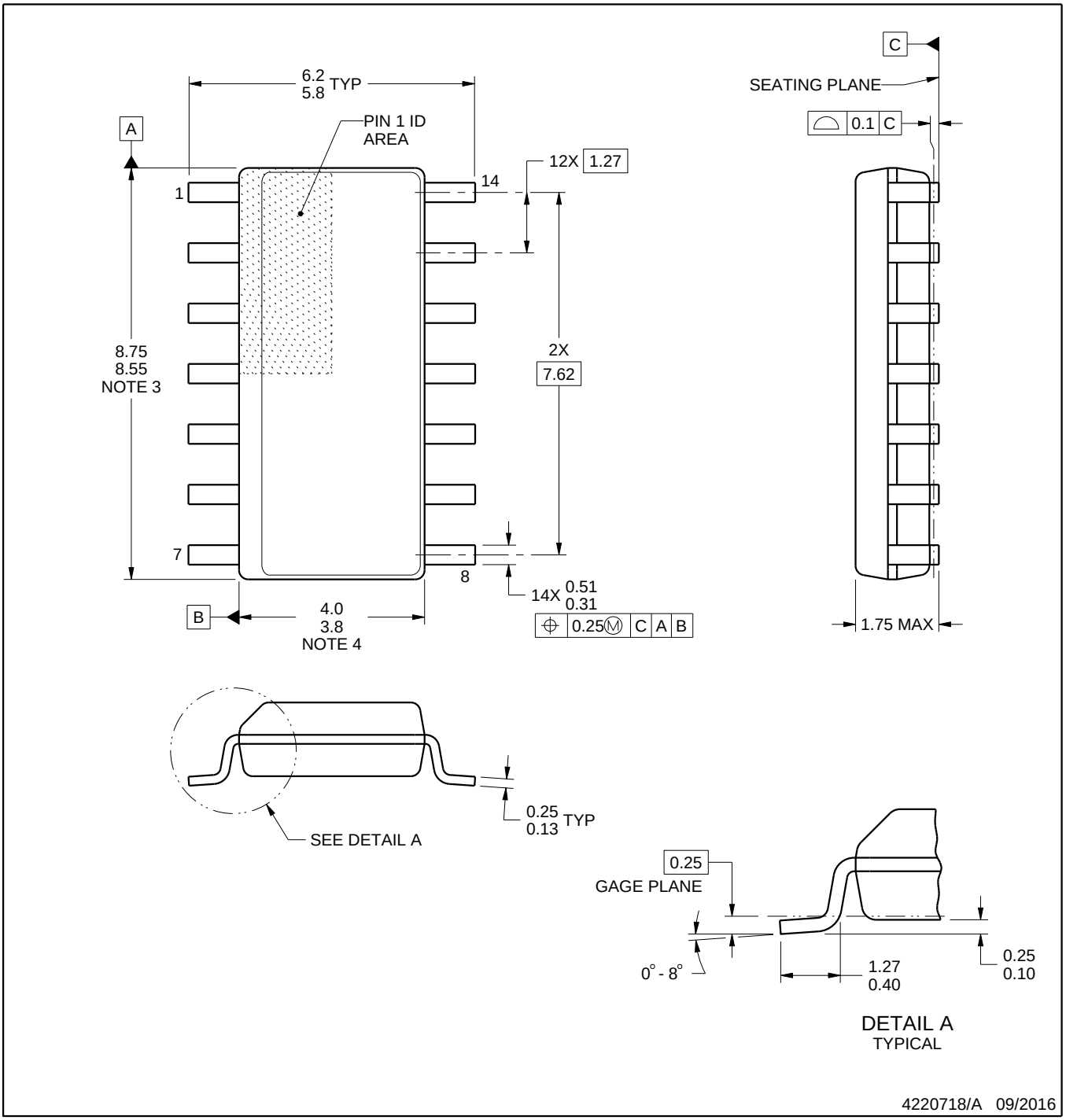


PACKAGE OUTLINE

D0014A

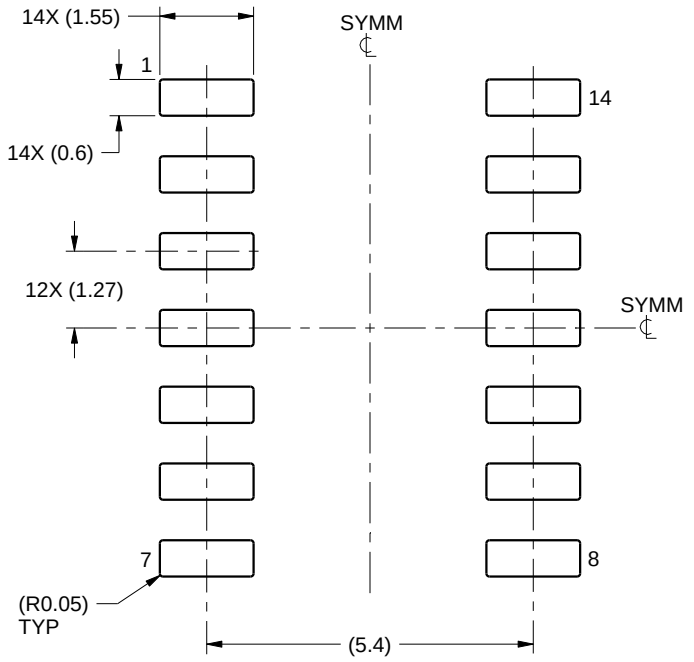
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

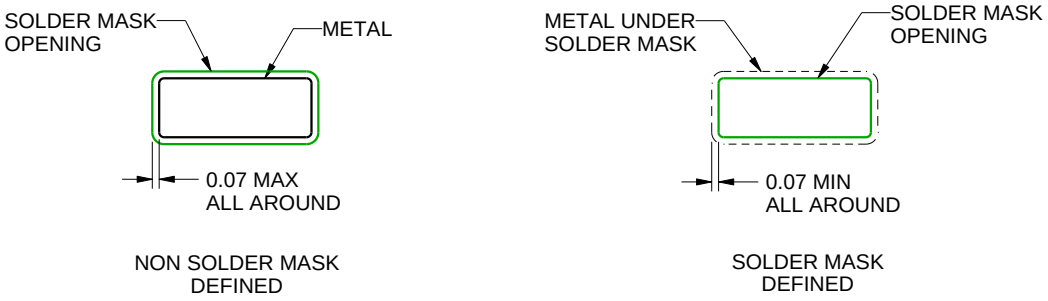


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

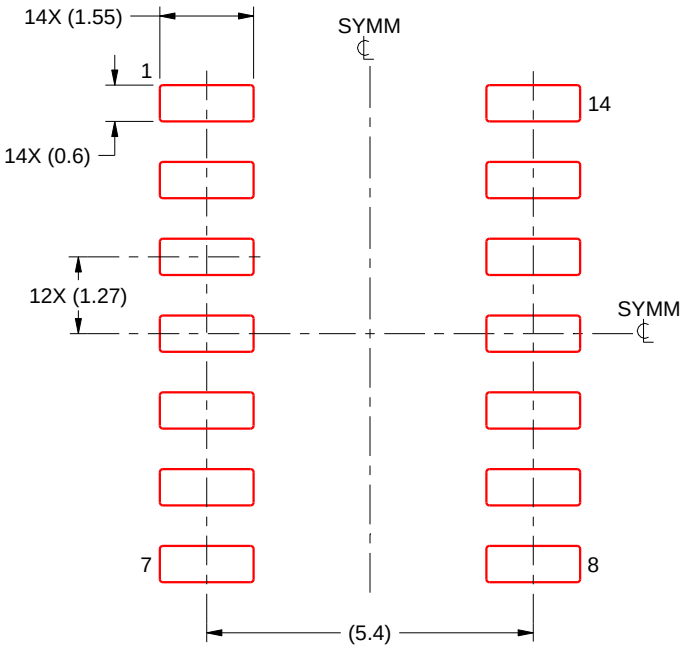
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

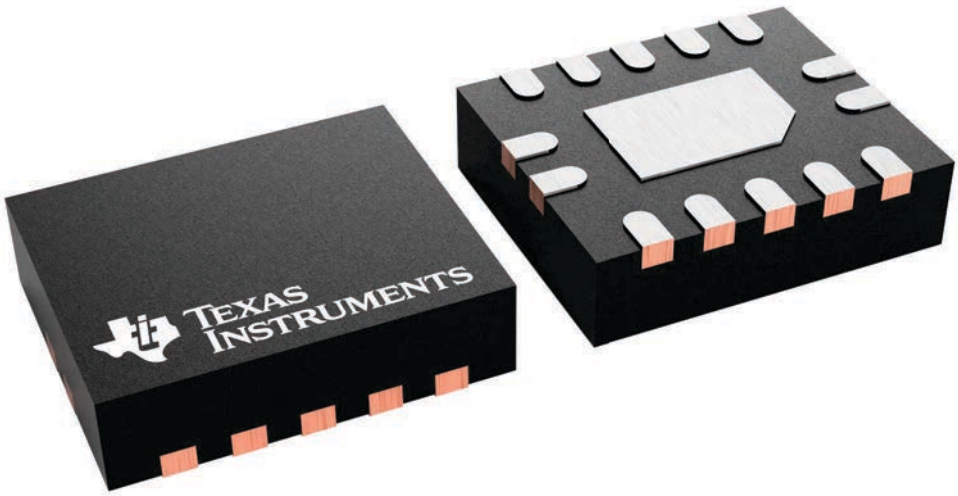
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

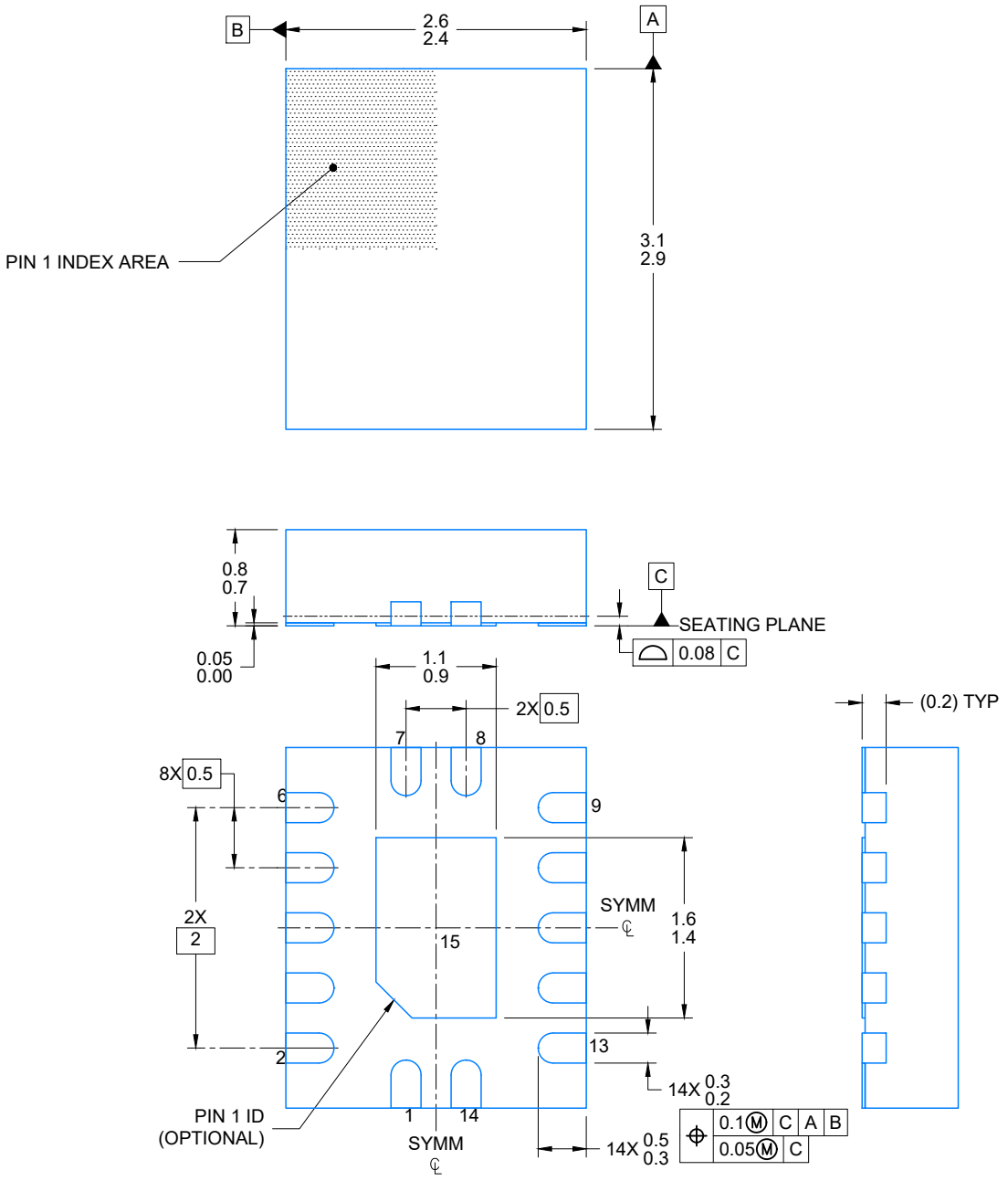


PACKAGE OUTLINE

BQA0014A

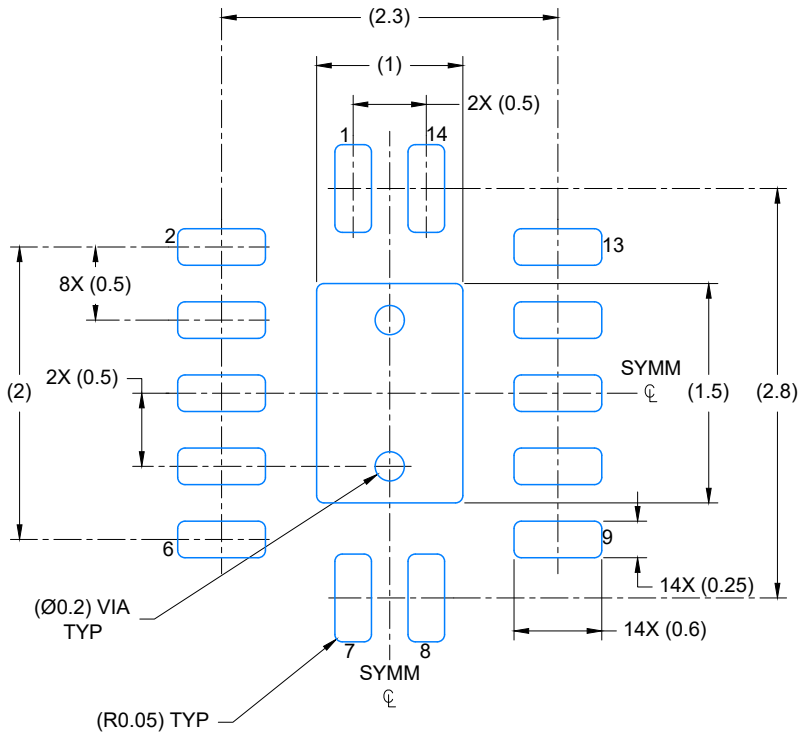
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

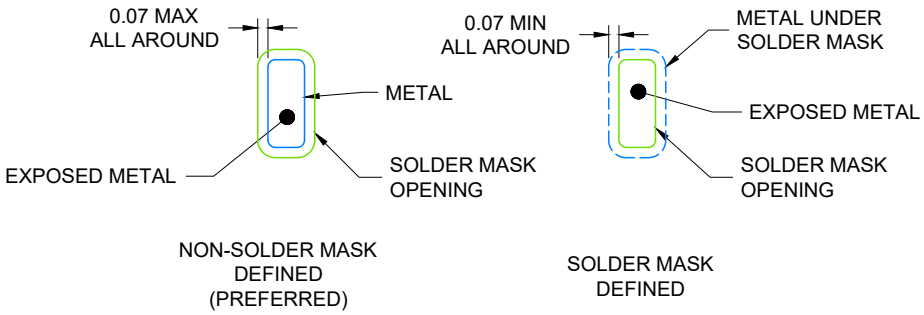


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



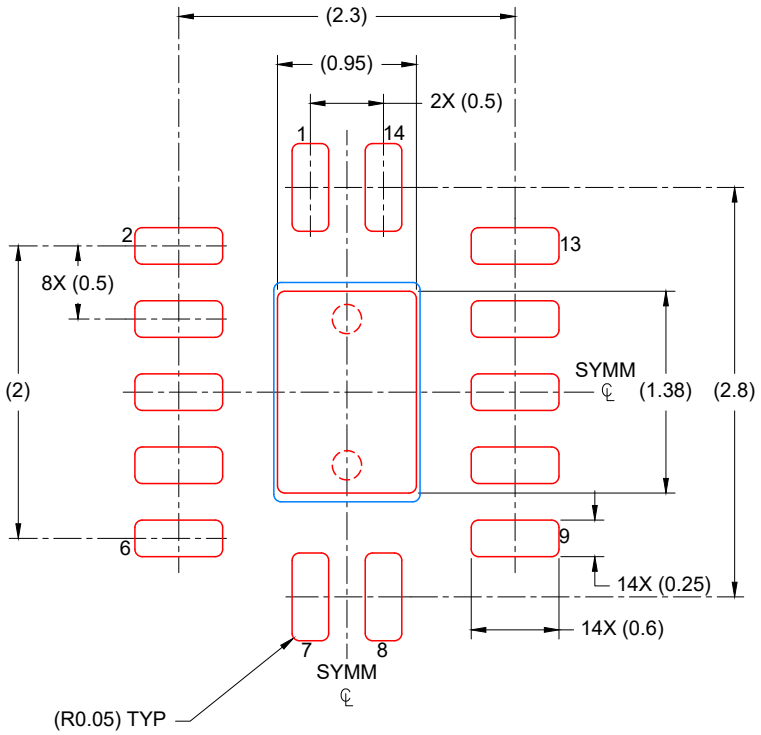
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

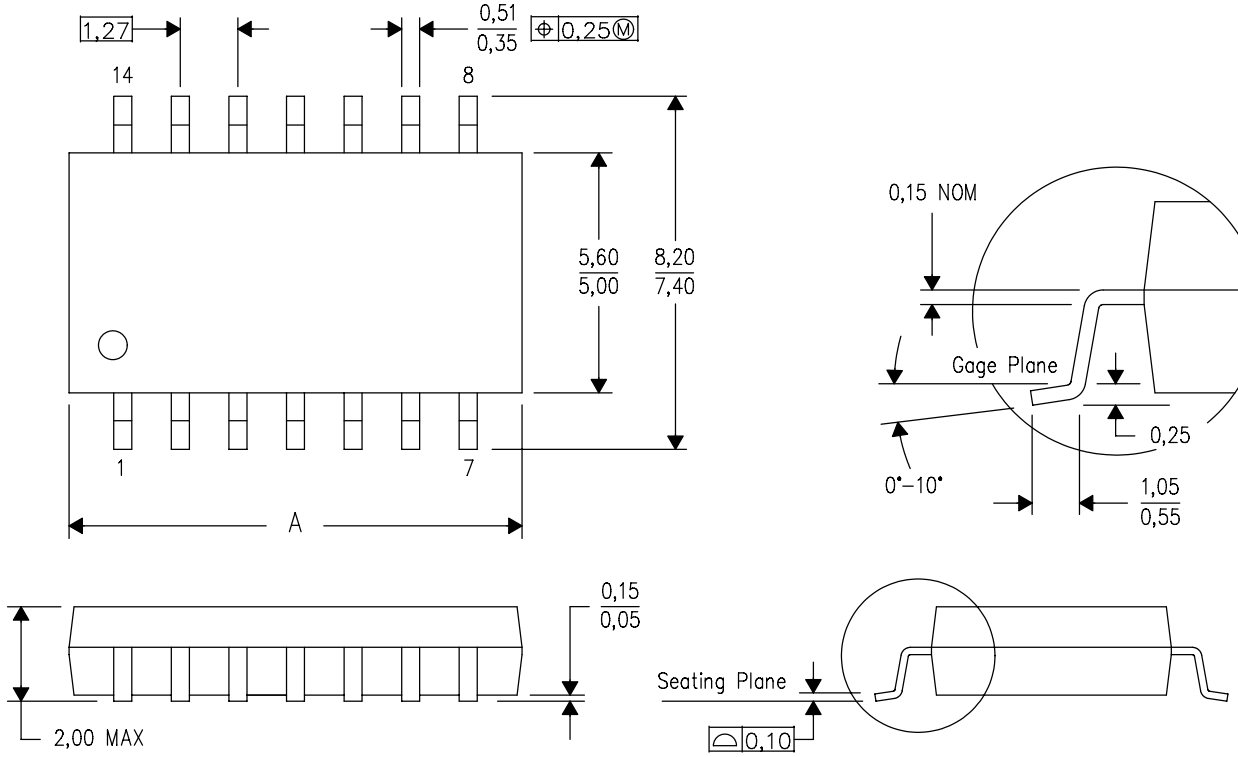
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

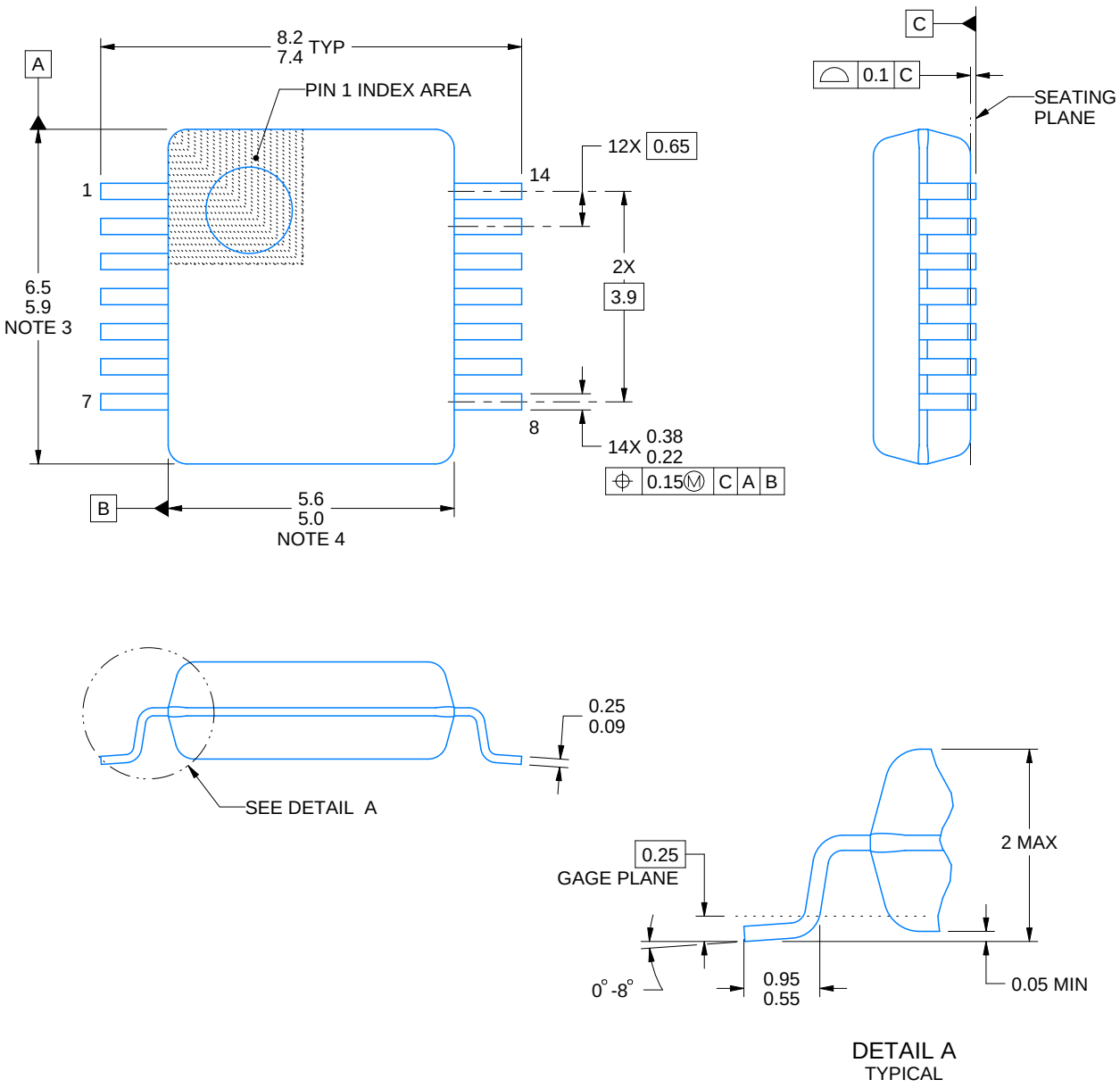
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

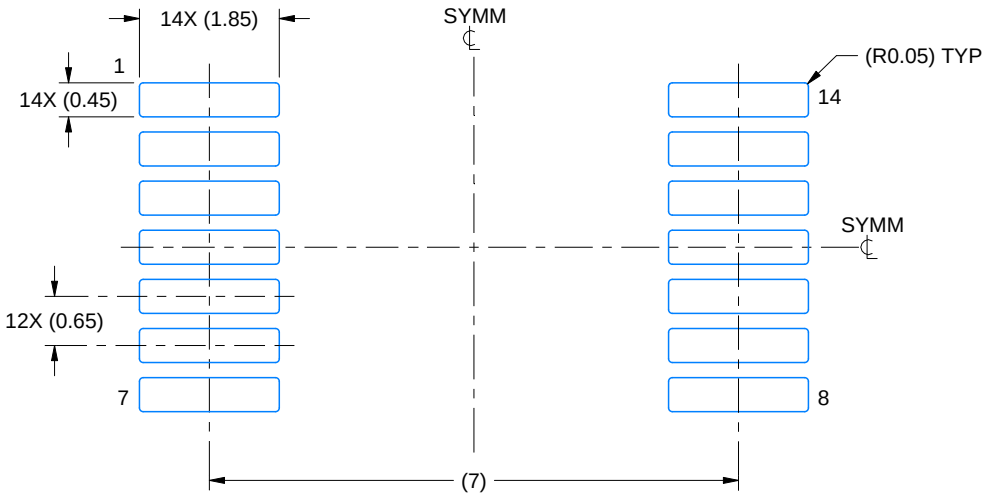
SMALL OUTLINE PACKAGE



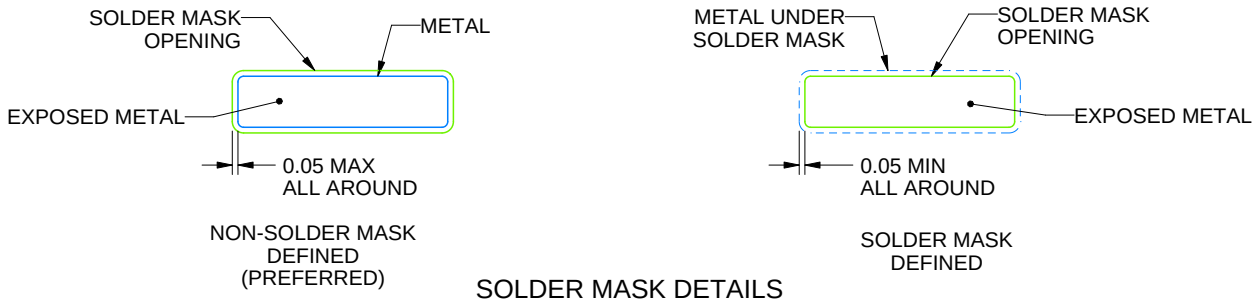
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

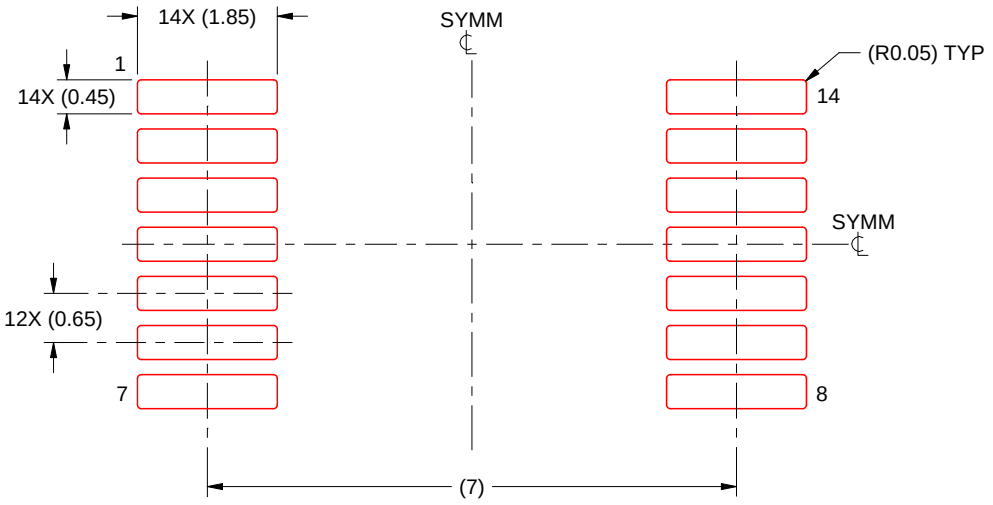


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

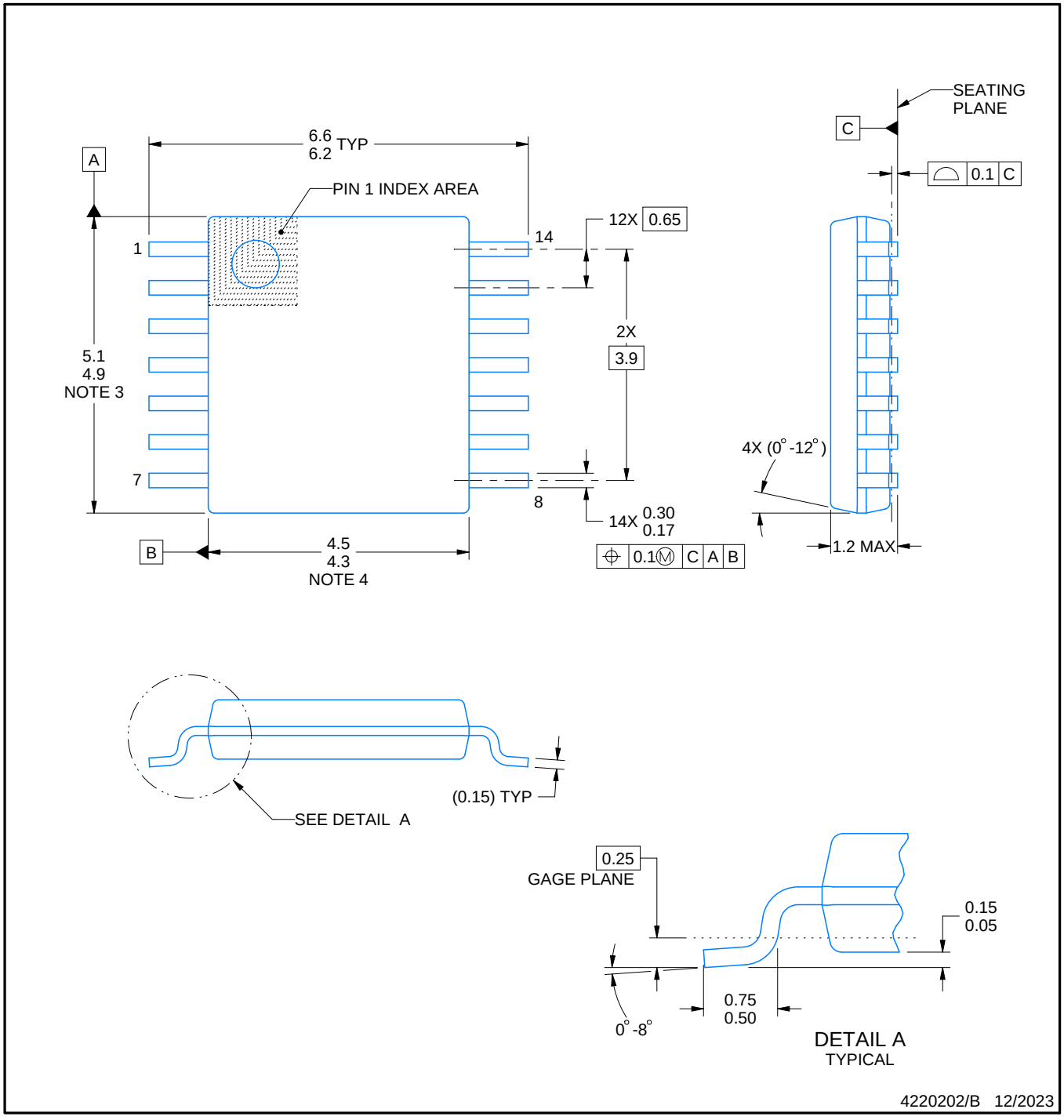
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

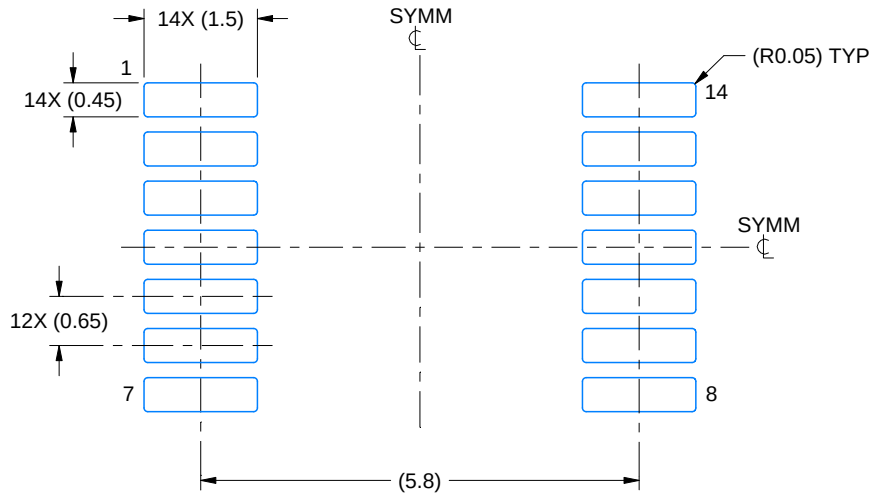
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

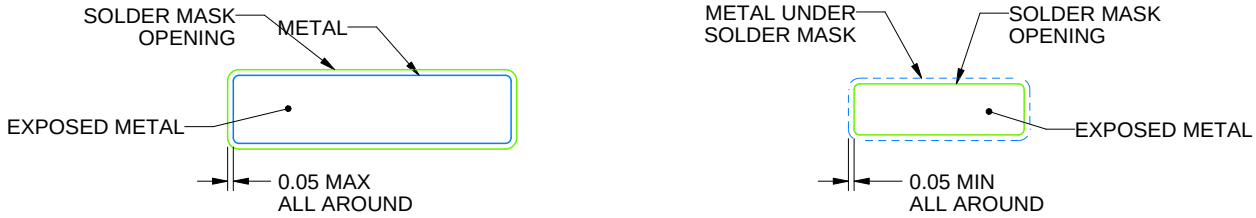


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

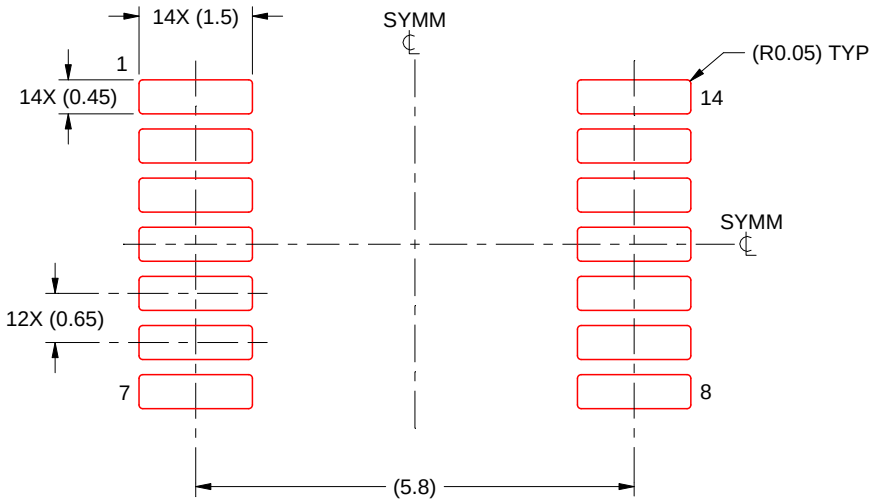


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月